IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Patent Application No. 09/449,912

Applicant: Divittorio

Filed: December 2, 1999

TC/AU: 2195

Examiner: Kenneth Tang

Docket No.: 202232 (Client Reference No. 99,032 US)

Customer No.: 23460

APPELLANT'S APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In support of the appeal from the Office Action dated October 6, 2006, Appellant submits this Appeal Brief.

Real Party In Interest

The patent application that is the subject of this appeal is assigned to The Foxboro Company.

Related Appeals and Interferences

There are no appeals or interferences that are related to this appeal.

Status of Claims

Claims 1-26 stand finally rejected, and these rejections are presently being appealed.

A complete listing of the presently pending claims appears in the Claims Appendix.

Status of Amendments

There were no amendments submitted after the rejection from which this appeal was taken.

Summary of Claimed Subject Matter

Claims 1-26, including independent **claims 1, 13, 25 and 26** are pending. The summaries of the independent claims reference the specification and drawings filed with the application on December 2, 1999.

Independent **claim 1** pertains to a control processor for executing a set of control tasks defining dynamic model-based interactive control of an industrial process. See, generally, FIG. 2, control processor 102, page 6, lines 12-28. In accordance with the claimed invention, the control processor includes an embedded control task comprising a multivariable linear program including a set of output values corresponding to process setpoints. See, e.g., Multivariable control application 138, page 11, lines 5-27. The multivariable linear program operates to generate, for example, a set of setpoints for a controlled industrial process that optimizes operation of an industrial process given a set of input values including costs and operational constraints.

The control processor also executes a set of control blocks including regulatory control blocks having output values that are transmitted by the control processor to field devices coupled to the industrial process. See, e.g., Control blocks 124, 126, 128, 130, 134, page 7, line 29 et seq.

The embedded control task executes at a lower execution priority than an execution priority of the set of control blocks. See, e.g., page 14, lines 11-21. In the illustrative embodiment, the embedded multivariable control application 138, which provides process setpoints for use by, for example, regulatory control blocks, executes within the control processor 102 at a lower priority than the control blocks including the regulatory control block 130, input block 124, and output block 134.

Independent **claim 13** recites a method for operating a control processor (e.g., Control Processor 2, 102 in Figs. 1a-1b, 2 and 3), in an industrial process control environment (See, e.g., FIGs. 1a-1b and associated written description), to establish operating values including a set of setpoint values (e.g., setpoints for regulatory control block 130) and a set of process control

variables (e.g., signal 122 provided by output block 134) associated with control elements in a controlled industrial process based upon a set of input variables (e.g., signals 120 received by input blocks 124, 126 and 128) including process variables provided to the control processor and representing the present state of the controlled industrial process. The general arrangement of the control processor and its executable components are described in detail with reference to FIG. 3 at page 7, line 24 to page 11, line 27.

The recited steps of the method of claim 13 are generally described with reference to an exemplary embodiment summarized in FIG. 5 wherein the embedded multivariable control application (application 138) operates in the background at a lower (interrupted) priority to the cyclically executed control blocks. The disclosed/claimed method of control processor operation thus includes executing, by the control processor, an embedded multivariable control application including computer instructions facilitating computing a setpoint value corresponding to a process control variable. See, e.g., step 312, page 16, lines 20-28. The method also includes executing, by the control processor, a set of control blocks including regulatory control blocks for receiving and storing a set of process variables representing the present state of a controlled process. See, e.g., step 310, page 16, lines 13-20; and description of control blocks with reference to FIG. 3.

In accordance with the claimed invention, and as shown in FIG. 5, the embedded multivariable control application (e.g., application 138) executes at a lower execution priority (as a background task resumed, for example during step 312) than an execution priority of the set of control blocks that are executed in the foreground until completed during step 310.

Independent **claim 25** is directed to an industrial process control computer having multiple operating levels. See, e.g., Control Processor 2 and Control Processor 102; and FIGs. 1a-1b, 2, and 3. The control processor includes a background control program execution level wherein the process control computer executes an embedded multivariable process control application including instructions for executing a multivariable linear program to generate a set of values corresponding to process control variable setpoints. See, e.g., Multivariable control application 138, page 11, lines 5-27; and FIG. 5, step 312, page 16, lines 20-28.

The control process also includes a foreground control block execution level wherein the process control computer executes a set of control blocks, at a higher execution priority level

than the background control program execution level, the set of control blocks including program instructions that, when executed, receive and store a set of process variable values representing the state of a controlled process. See, e.g., Control blocks 124, 126, 128, 130, 134, page 7, line 29 et seq.; and FIG. 5, steps 300-312, page 16, lines 13-20.

Independent **claim 26** recites a multi-level multivariable industrial process control program execution framework for an industrial control processor. The arrangement is generally disclosed with reference to FIGs. 3 (description of executable components) and 5 (method of implementing execution of the two identified categories of executable components). The execution framework includes a first cyclically executed sequence of instructions, repeatedly executed according to a first configurable repetition period and at a first level of execution priority. See, Embedded App Cycle discussed at steps 302-308 of FIG. 5, page 15, line 25 to 33. The first cyclically executed sequence of instructions includes at least a set of instructions for calculating a setpoint value for a process control variable. See, e.g., control application 138, page 11, lines 5-27.

The execution framework recited in claim 26 includes a second cyclically executed sequence of instructions, repeatedly executed according to a second repetition period and at a second level of execution priority. See, e.g., FIG. 5, page 14, lines 22-32. The second level of execution priority exceeds the first level of execution priority, and the control processor temporarily suspends executing the first cyclically executed sequence of instructions in order to execute the second cyclically executed sequence of instructions. See, FIG. 5, step 300, page 15, lines 1-15.

Grounds of Rejection to be reviewed on Appeal

The grounds of rejection to be reviewed on appeal are the grounds stated in the Office Action mailed on October 6, 2006. In particular, Appellant appeals the Office Action's:

1. Rejection of Claims 1-7, 13-19, and 25-26 as obvious under 35 U.S.C. Section 103(a) over Applicant's Admitted Prior Art (AAPA) in view of Sinibaldi et al., U.S. Patent No. 6,549,945 (Sinibaldi); and

2. Rejection of Claims 8-12 and 20-24 as obvious under 35 U.S.C. Section 103(a) over AAPA in view of Sinibaldi and Messih et al. U.S. Patent No. 5,526,794 (Messih).

Argument

Appellant requests reversal of the rejection of presently pending claims 1-26 (provided in the Claims Appendix attached hereto). The invention recited in the each of the independent claims is directed to a particular way in which a single control processor executes: (1) an embedded control task comprising a multivariable linear program for establishing setpoints for a controlled process, and (2) a set of control blocks that provide output values for field devices. In contrast to known control processors, the claimed embedded control task is executed on the control processor rather than receiving the setpoints from a networked computer, and the claimed embedded control task is executed at a relatively low priority in comparison to the set of control blocks on the control processor. Nowhere does the prior art (including the cited Sinibaldi patent) provide a reason for implementing this specific multi-level control program execution scheme. Therefore the claimed invention would not have been obvious to one skilled in the art at the time of the invention.

The grounds for Appellant's appeal are addressed further herein below.

Rejection of Claims 1-7, 13-19 and 25-26 as Obvious over AAPA in view of Sinibaldi

Claims 1, 6, 7, 13, 18, 19, 25 and 26

Appellant appeals the rejection of independent **claim 1** as being obvious over AAPA in view of Sinibaldi because the prior art does not support modification of AAPA in view of Sinibaldi to render Appellant's claimed invention. In fact, while executing different program components at different priority levels on a same computer system were indeed known at the time of the invention, there was no reason or teaching for the specific execution scheme recited in claim 1 wherein a multivariable linear program executes at a relatively low priority than a set of control blocks on a control processor for an industrial process control system.

Appellant submits that there is an absence of any reason for one skilled in the art at the time of the invention to modify Applicant's Admitted Prior Art by incorporating the embedded control task comprising a multivariable linear program into a control processor, *and* executing the embedded control task at a lower priority than the set of control blocks. The Office Action, from which Appellant's appeal was taken, asserts that Sinibaldi, at column 18, lines 25-28, teaches "having a matrix which represents a multivariable linear program, wherein the entries of

the matrix are setpoints." However, Sinibaldi's "Matrix" described at column 18 refers to a "table" (i.e., an array) in memory. Nowhere does Sinibaldi disclose that the contents of the table are generated from a multivariable linear program. It necessarily follows that Sinibaldi does not disclose that the multivariable linear program operates at a lower execution priority than an execution priority of a set of control blocks. Thus, the premise upon which the Office Action's rejection of claim 1 relies is unsupported by the actual teachings of Sinibaldi.

Furthermore, Appellant traverses the Office Action's stated motivation for modifying AAPA in view of Sinibaldi since there is no reasonable expectation that some benefit would arise from *executing a multivariable linear program on a control processor at a relatively lower priority that the control block execution task.* To the contrary, the computational burden placed by the multivariable linear program on the control processor could limit the control processor's ability to perform other desired functions. By placing both block processing and linear program execution on a same control processor one runs the risk that neither process control system component will operate in a satisfactory manner. Thus, contrary to the Office Action's assertion, the claimed invention would, if anything, tend to reduce "flexibility."

Finally, the prior art does not disclose or provide a reason to modify AAPA such that the control processor executes the specifically recited control block/multivariable linear program execution scheme recited in claim 1. There are virtually limitless arrangements for assigning priorities, if at all, between control block execution and multivariable linear program execution. In fact, one might even consider the disclosed and claimed arrangement to be overly restrictive. There is no teaching in the prior art that the particular claimed execution arrangement is desirable or even feasible.

Appellant requests reversal of the rejection of claim 1 because the rejection does not show proper support/reasons to modify Applicant's admitted prior to render the control processor execution scheme recited in claim 1. Executing various program tasks at different priority levels was indeed well known at the time of the invention. However, nowhere does the prior art teach, suggest, motivate, or otherwise provide a reason for one skilled in the art at the time the application was filed to incorporate the embedded multivariable linear program that calculates set point values for the control processor into the process controller and execute the multivariable application program at a lower assigned priority than a set of control blocks. For at least this

reason the presently pending claim 1 is non-obvious over the prior art presently known to Appellant.

The recited elements of independent method claim 13 and independent apparatus/system claims 25 and 26 are similar to those recited in claim 1. Appellant's remarks relating to claim 1 are applicable to the Office Action's rejection of claims 13, 25 and 26.

Claim 2-3, 5, 14, and 17

Appellant requests reversal of the rejection of claims 2, 3, 5, 14, and 17 for at least the further reason that, notwithstanding the existence of supervisory control blocks in the prior art, there is no teaching to execute them in the multi-level execution scheme recited in claim 1 along with regulatory control blocks. In the event that the rejection is not withdrawn, Appellant requests identification of a reason why, in view of the prior art teachings, one skilled in the art would have implemented a control processor execution scheme that embodied the limitations recited in each of these claims.

Claims 4 and 16

Appellant requests reversal of the rejection of claims 4 and 16 for at least the reason that the prior art does not even remotely teach the use of a multivariable control block to download a process control model for implementation by the embedded control task. In fact, the prior art does not even disclose the recited embedded control task, on the control processor, which comprises the multivariable linear program.

Claim 15

Appellant requests reversal of the rejection of claim 15 for at least the reason that the prior art does not even remotely suggest the recited step of downloading data from a workstation to a database accessed by a multivariable control block. In the event the rejection is not withdrawn, Appellant specifically requests identification of the teachings of the prior art upon which the rejection relies.

Rejection of Claims 8-12 and 20-24 as Obvious over AAPA in view of Sinibaldi and Messih

Notwithstanding Appellant's specific previous requests, the Office Action rejects claims 8-12 and 20-24 without identifying the recited elements in the prior art reference and explaining the basis for combining the elements to render Appellant's claimed invention. More particularly, the Office Action does not explain how the teachings of Messih et al. apply to the specific multi-level control program execution scheme (including an embedded task and a set of control blocks operating at different priorities) recited in each of the claims. Furthermore, Appellant traverses the application of Messih's teachings regarding a car engine to the present invention which is directed to a control program execution scheme for an industrial process (potentially having several orders of magnitude greater numbers of variables than a car engine control program).

In the event that the rejections of claims 8-12 and 20-24 are not withdrawn/reversed, Appellant respectfully requests identification of the specific portions of the cited references corresponding to the recited claim elements. Further specific comments are provided herein below with reference to claims 8-9, 11-12, 20-21, and 23-24.

Claims 8, 11, 20 and 23

Appellant requests reversal of the rejection of claims 8, 11, 20 and 23. Each of these claims recites a repetition cycle parameter for the embedded control task (as opposed to the control block processing cycle). The Office Action does not identify where any of the cited references specifies a repetition cycle parameter associated with the embedded (low priority task). The claimed repetition period for the embedded task is distinguished from the repetition period of the set of control blocks (high priority task).

Claims 9 and 21

Appellant requests reversal of the rejection of claims 9 and 21. The prior art neither discloses nor suggests the claimed supervisory control block, within the set of control blocks (operating at the higher priority), that controls commencing a repetition cycle of the embedded (lower priority) task. This element is clearly not present in AAPA and is not even remotely suggested by Sinibaldi or Messih.

Claims 12 and 24

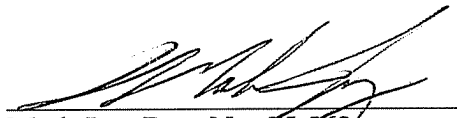
Appellant requests reversal of the rejection of claims 12 and 24 since none of the cited references discloses or suggests an embedded repetition period exceeding a block processing cycle period.

Conclusion

The Office Action has not set forth a *prima facie* case of obviousness for the rejection of the presently pending claims 1-26. Appellant submits that the prior art neither discloses nor suggests modifying AAPA to render the claimed multi-level control task execution scheme wherein an embedded multivariable linear program, that provides setpoints for an industrial process, executes on a control processor at a lower execution priority level than a set of control blocks.

For this and other reasons submitted herein above, Appellant requests reversal of the presently pending rejection of claims 1-26.

Respectfully submitted,



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Claims Appendix

1. (Previously presented) A control processor for executing a set of control tasks defining dynamic model-based interactive control of an industrial process, the control processor comprising:

an embedded control task comprising a multivariable linear program including a set of output values corresponding to process setpoints; and

a set of control blocks including regulatory control blocks having output values that are transmitted by the control processor to field devices coupled to the industrial process, wherein the embedded control task executes at a lower execution priority than an execution priority of the set of control blocks.

2. (Original) The control processor of claim 1 wherein the set of control blocks comprise supervisory control blocks.

3. (Original) The control processor of claim 2 wherein the supervisory control blocks include a multivariable control block including computer instructions facilitating communication of data between the control processor and a workstation.

4. (Original) The control processor of claim 3 wherein the multivariable control block includes computer instructions for receiving and storing a process control model to be implemented by the embedded control task.

5. (Original) The control processor of claim 2 wherein the supervisory control blocks include at least one multivariable loop block including computer instructions for providing an input value for a regulatory control block.

6. (Previously presented) The control processor of claim 5 wherein the regulatory control block is a proportional-integral-derivative block.

7. (Original) The control processor of claim 5 wherein the regulatory control block is a ratio block.

8. (Previously presented) The control processor of claim 1 further comprising a repetition cycle parameter specifying a period for re-commencing a cycle of the embedded control task.

9. (Original) The control processor of claim 8 wherein the set of control blocks includes a supervisory control block including a sequence of instructions to determine when to re-commence a cycle of the embedded task in accordance with a value specified by the repetition cycle parameter.

10. (Original) The control processor of claim 1 further comprising a block processing cycle parameter specifying a repetition period for re-commencing a cycle of executing the set of control blocks.

11. (Original) The control processor of claim 10 further comprising a repetition cycle parameter specifying a period for re-commencing a cycle of executing the embedded control task.

12. (Original) The control processor of claim 11 wherein a period specified by the repetition cycle parameter exceeds a period specified by the block processing cycle parameter.

13. (Previously presented) A method for operating a control processor, in an industrial process control environment, to establish operating values including a set of setpoint values and a set of process control variables associated with control elements in a controlled industrial process based upon a set of input variables including process variables provided to the control processor and representing the present state of the controlled industrial process, the method comprising the steps of:

executing, by the control processor, an embedded multivariable control application including computer instructions facilitating computing a setpoint value corresponding to a process control variable; and

executing, by the control processor, a set of control blocks including regulatory control blocks for receiving and storing a set of process variables representing the present state of a controlled process, wherein the embedded multivariable control application executes at a lower execution priority than an execution priority of the set of control blocks.

14. (Original) The method of claim 13 wherein the set of control blocks comprise supervisory control blocks.

15. (Original) The method of claim 14 wherein the supervisory control blocks include a multivariable control block and further including the step of downloading data from a workstation to a database accessed by the multivariable control block.

16. (Original) The method of claim 15 further comprising the steps of receiving and storing, within the database accessed by the multivariable control block, a process control model to be implemented by the embedded multivariable control application.

17. (Original) The method of claim 14 wherein the supervisory control blocks include at least one multivariable loop block, and further comprising the step of providing an input value for a regulatory control block in accordance with execution of instructions and data associated with the at least one multivariable loop block.

18. (Previously presented) The method of claim 17 wherein the regulatory control block is a proportional-integral-derivative block.

19. (Original) The method of claim 17 wherein the regulatory control block is a ratio block.

20. (Previously presented) The method of claim 13 further comprising the step of maintaining a repetition cycle parameter specifying a period for re-commencing a cycle of the embedded multivariable control application.

21. (Original) The method of claim 20 wherein the set of control blocks includes a supervisory control block, and further comprising the step of determining, by the supervisory control block, when to re-commence a cycle of the embedded multivariable control application in accordance with a value specified by the repetition cycle parameter.

22. (Original) The method of claim 13 further comprising the step of maintaining a block processing cycle parameter specifying a repetition period for re-commencing a cycle of executing the set of control blocks.

23. (Previously presented) The method of claim 22 further comprising the step of maintaining a repetition cycle parameter specifying a period for re-commencing a cycle of executing the embedded multivariable control application.

24. (Original) The method of claim 23 wherein a period specified by the repetition cycle parameter exceeds a period specified by the block processing cycle parameter.

25. (Previously presented) An industrial process control computer having multiple operating levels including:

a background control program execution level wherein the process control computer executes an embedded multivariable process control application, the embedded control application including instructions for executing a multivariable linear program to generate a set of values corresponding to process control variable setpoints; and

a foreground control block execution level wherein the process control computer executes a set of control blocks, at a higher execution priority level than the background control program execution level, the set of control blocks including program instructions that, when executed, receive and store a set of process variable values representing the state of a controlled process.

26. (Previously presented) A multi-level multivariable industrial process control program execution framework for an industrial control processor including:

a first cyclically executed sequence of instructions, repeatedly executed according to a first configurable repetition period and at a first level of execution priority, the first cyclically executed sequence of instructions including at least a set of instructions for calculating a setpoint value for a process control variable; and

a second cyclically executed sequence of instructions, repeatedly executed according to a second repetition period and at a second level of execution priority, the second level of execution priority exceeding the first level of execution priority, and thus enabling the control processor to temporarily suspend execution of the first cyclically executed sequence of instructions in order to execute the second cyclically executed sequence of instructions.

Evidence Appendix

NOT APPLICABLE

Related Proceedings Appendix

NOT APPLICABLE